10-2-00 A

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PTO/SB/05 (2/98)
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UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Attorney Docket No.	042390.P6126D
First Inventor or Application Identifier	Makarem A. Hussein
Title	A PROCESS TO MANUFACTURE CONTINUOUS METAL INTERCONNECTS
Express Mail Label No.	EL635878149US

APPLICATION ELEMENTS
See MPEP chapter 600 concerning utility patent application contents

ADDRESS TO: Assistant Commissioner for Patents
Box Patent Application
Washington, DC 20231

1. [X] Fee Transmittal Form *(e.g. PTO/SB/17)*
(Submit an original, and a duplicate for fee processing)
2. [X] Specification Total Pages 20
(preferred arrangement set forth below)
- Descriptive title of the Invention
- Cross References to Related Applications
- Statement Regarding Fed sponsored R & D
- Reference to Microfiche Appendix
- Background of the Invention
- Brief Summary of the Invention
- Brief Description of the Drawings *(if filed)*
- Detailed Description
- Claim(s)
- Abstract of the Disclosure

3. [X] Drawing(s) *(35 U.S.C.113)* Total Sheets 2
4. Oath or Declaration Total Pages 2
   a. [ ] Newly executed (original copy)
   b. [X] Copy from a prior application (37 CFR 1.63(d))
   (for continuation/divisional with Box 16 completed)
      i. [ ] DELETION OF INVENTOR(S)
      Signed statement attached deleting inventor(s) named in the prior application, see 37 CFR 1.63(d)(2) and 1.33(b).

NOTE FOR ITEMS 1 & 13: IN ORDER TO BE ENTITLED TO PAY SMALL ENTITY FEES, A SMALL ENTITY STATEMENT IS REQUIRED (37 C.F.R. § 1.27), EXCEPT IF ONE FILED IN A PRIOR APPLICATION IS RELIED UPON (37 C.F.R. § 1.28).

5. [ ] Microfiche Computer Program *(Appendix)*
6. Nucleotide and/or Amino Acid Sequence Submission *(if applicable, all necessary)*
   a. [ ] Computer Readable Copy
   b. [ ] Paper Copy (identical to computer copy)
   c. [ ] Statement verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

7. [ ] Assignment Papers (cover sheet & document(s))
8. [ ] 37 CFR 3.73(b) Statement [ ] Power of Attorney
(when there is an assignee)
9. [ ] English Translation Document *(if applicable)*
10. [X] Information Disclosure Statement (IDS)/PTO - 1449 [ ] Copies of IDS Citations
11. [X] Preliminary Amendment
12. [X] Return Receipt Postcard (MPEP 503)
(Should be specifically itemized)
13. [ ] *Small Entity Statement(s) [ ] Statement filed in prior application, Status still proper and desired
14. [ ] Certified Copy of Priority Document(s)
(if foreign priority is claimed)
15. [ ] Other: . . . . . .

16. If a CONTINUING APPLICATION, *check appropriate box, and supply the requisite information below and in a preliminary amendment:*

[ ] Continuation [X] Divisional [ ] Continuation-in-part (CIP) of prior application No: 09 / 163,847

Prior application Information: Examiner Schillinger, L. Group/Art Unit: 2813

For CONTINUATION or DIVISIONAL APPS only: The entire disclosure of the prior application, from which an oath or declaration is supplied under Box 4b, is considered a part of the disclosure of the accompanying continuation or divisional application and is hereby incorporated by reference. The incorporation can only be relied upon when a portion has been inadvertently omitted from the submitted application parts.

17. CORRESPONDENCE ADDRESS

[ ] *Customer Number of Bar Code Label* *(Insert Customer No. or Attach bare code label here)* or [X] *Correspondence address below*

Name	BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP				
Address	12400 Wilshire Boulevard, Seventh Floor				
City	Los Angeles	State	California	Zip Code	90025
Country	U.S.A.	Telephone	(310) 207-3800	Fax	(310) 820-5988

Name (Print/Type)	William Thomas Babbitt, Reg. No. 39,591
Signature	William T Babbitt — Date 9/28/00

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FEE TRANSMITTAL

Petent fees are subject to annual revision on October 1. These are the fees effective October 1, 1997. Small Entity payments must be supported be a small entity statement, otherwise large entity fees must be paid. See Forms PTO/SB/09-12. See 37 C.F.R. §§ 1.28 and 1.28

TOTAL AMOUNT OF PAYMENT ($) 690.00

Complete if Known	
Application Number	
Filing Date	
First Named Inventor	Makarem A. Hussein
Examiner Name	
Group Art Unit	
Attorney Docket Number	042390.P6126D

METHOD OF PAYMENT (check one)

1. ☒ The Commissioner is hereby authorized to charge indicated fees and credit any over payments to:

Deposit Account Number: 02-2666

Deposit Account Name: Blakely, Sokoloff, Taylor & Zafman LLP

☒ Charge Any Additional Fee Required Under 37 CFR 1.16 and 1.17

2. ☒ Payment Enclosed:

☒ Check ☐ Money Order ☐ Other

FEE CALCULATION (fees effective 10/01/96)

1. FILING FEE

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
101	690	201	345	Utility filing fee	$690
106	310	206	155	Design filing fee	
107	480	207	240	Plant filing fee	
108	690	208	345	Reissue filing fee	
114	150	214	75	Provisional filing fee	

SUBTOTAL (1) ($) 690.00

2. EXTRA CLAIM FEES

	Extra Claims		Fee from below		Fee Paid
Total Claims 3	-20** = 0	X	$18.00	=	0.00
Independent Claims 1	-3** = 0	X	$78.00	=	0.00
Multiple Dependent				=	

***or number of previously paid, if greater; For Reissues, see below*

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description
103	18	203	9	Claims in excess of 20
102	78	202	39	Independent claims in excess of 3
104	270	204	135	Multiple Dependent claim
109	78	209	39	**Reissue independent claims over original patent
110	18	210	9	**Reissue claims in excess of 20 and over original patent

SUBTOTAL (2) ($) 0.00

FEE CALCULATION (continued)

3. ADDITIONAL FEE

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
105	130	205	65	Surcharge - late filing fee or oath	
127	50	227	25	Surcharge - late provisional filing fee or cover sheet.	
139	130	139	130	Non-English specification	
147	2,520	147	2,520	For filing a request for reexamination	
112	920*	112	920*	Requesting publication of SIR prior to Examiner action	
113	1,840*	113	1,840*	Requesting publication of SIR after Examiner action	
115	110	215	55	Extension for response within first month	
116	380	216	190	Extension for response within second month	
117	870	217	435	Extension for response within third month	
118	1,360	218	680	Extension for response within fourth month	
128	1,850	228	925	Extension for response within fifth month	
119	300	219	150	Notice of Appeal	
120	300	220	150	Filing a brief in support of an appeal	
121	260	221	130	Request for oral hearing	
138	1,360	138	1,360	Petition to institute a public use proceeding	
140	110	240	55	Petition to revive - unavoidably	
141	1,210	241	605	Petition to revive - unintentionally	
142	1,210	242	605	Utility issue fee (or reissue)	
143	430	243	215	Design issue fee	
144	580	244	290	Plant issue fee	
122	130	122	130	Petitions to the Commissioner	
123	50	123	50	Petitions related to provisional applications	
126	240	126	240	Submission of Information Disclosure Stmt	
581	40	581	40	Recording each patent assignment per property (times number of properties)	
146	760	246	380	Filing a submission after final rejection (37 CFR 1.129(a))	
149	760	249	380	For each additional invention to be examined (37 CFR 1.129(b))	
Other fee (specify)					
Other fee (specify)					

* Reduced by Basic Filing Fee Paid

SUBTOTAL (3) ($)

SUBMITTED BY				Complete (if applicable)	
Typed or Printed Name	William Thomas Babbitt, Reg. No. 39,591			Reg. Number	
Signature	William T Babbitt	Date	9/29/00	Deposit Account User ID	02-2666

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Attorney's Docket No. 042390.P6126D
Express Mail No. EL635878149US

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

MAKAREM A. HUSSEIN

Serial No.

Filed:

For: *A Process to Manufacture Continuous Metal Interconnects*

Divisional Application of:
Serial No. 09/163,847
Filed: September 30, 1998

Examiner: Schillinger, L.

Art Unit 2813

PRELIMINARY AMENDMENT

Box New Patent Application
Assistant Commissioner for Patents
Washington, D.C. 20231

Dear Sir:

In connection with the filing of the Divisional Application under Rule 1.53(b), Applicant respectfully requests entry of the following amendments.

Please cancel claims 1-11.

In claim 12, line 5, please replace "a wall or walls" with --at least one wall--.

In claim 12, line 8, please replace "wall or walls" with --at least one wall--.

In claim 13, line 2, please replace "line" with --line.--.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN, LLP

Dated: 9/28/01

William Thomas Babbitt, Reg. No. 39,591

12400 Wilshire Boulevard
Seventh Floor
Los Angeles, California 90025
(310) 207-3800

Docket No. 042390.P6126
Express Mail No. EM560642969US

UNITED STATES PATENT APPLICATION

FOR

A PROCESS TO MANUFACTURE CONTINUOUS METAL INTERCONNECTS

Inventor:

MAKAREM A. HUSSEIN

Prepared by:

BLAKELY SOKOLOFF TAYLOR & ZAFMAN LLP
12400 Wilshire Boulevard, Seventh Floor
Los Angeles, California 90025
(310) 207-3800

BACKGROUND OF THE INVENTION

Field of the Invention

The invention relates to integrated circuit processing and, more particularly, to the patterning of interconnection lines on an integrated circuit.

Description of Related Art

Modern integrated circuits use conductive interconnections to connect the individual devices on a chip or to send and receive signals external to the chip. Popular types of interconnections include aluminum alloy interconnection lines and copper interconnection lines coupled to individual devices, including other interconnection lines, by interconnections through vias.

A typical method of forming an interconnection is a damascene process that involves forming a via and an overlying trench in a dielectric to an underlying circuit device, such as a transistor or an interconnection line. The via and trench are then lined with a barrier layer of a refractory material. Common refractory materials include titanium nitride (TiN) or tantalum (Ta). The barrier layer serves, in one aspect, to inhibit the diffusion of the interconnection material that will subsequently be formed in the via into the dielectric. Next, a suitable seed material is deposited on the wall or walls and base of the via. Suitable seed materials for the deposition of

copper interconnection material include copper and nickel. Next, interconnection material, such as copper, is deposited in a sufficient amount to fill the via and trench using, for example, an electroplating process. Thus, the interconnection formed in the via includes the barrier layer material since barrier layer material lines the base of the via.

A second method for forming an interconnection is described in the United States Patent Application Serial No. 09/001,349, filed December 31, 1997, assigned to Intel Corporation of Santa Clara, California, and titled "*A Single Step Electroplating Process for Interconnect Via Fill and Metal Line Patterning.*" That method includes forming a via in a dielectric to an underlying circuit device, such as a transistor or an interconnection line. The via and a top surface of the dielectric are then lined and covered with a barrier layer and a suitable seed material, respectively. A layer of photoresist or other masking material is then patterned over the seed material covering the top of the dielectric. An electroplating process is used to deposit a conductive material such as copper to fill the via and form an interconnection line over the dielectric according to the patterned masking material. The masking material and underlying conductive material is then removed. Once again, the interconnection formed in the via generally includes the barrier layer since barrier layer material lines the base of the via.

In general, the resistivity of the barrier layer material is much greater than the resistivity of copper. Thus, the inclusion of the barrier layer material at the base of the via and as part of the interconnection increases the resistivity of the interconnection. What is needed is an interconnection having reduced resistivity and a method of forming an interconnection with reduced resistivity compared to the prior art.

SUMMARY OF THE INVENTION

A method of forming an interconnection is disclosed. The method includes introducing a barrier material in a via of a dielectric to a circuit device on a substrate in such a manner to deposit the barrier material on the circuit device. A seed material is introduced into the via in manner that leaves the barrier material overlying the circuit device substantially exposed. The barrier material overlying the circuit device is substantially removed and a conductive material is introduced into the via to form the interconnection.

BRIEF DESCRIPTION OF THE DRAWINGS

The features, aspects, and advantages of the invention will become more thoroughly apparent from the following detailed description, appended claims, and accompanying drawings in which:

Figure 1 illustrates a cross-sectional side view of a portion of a substrate showing an interconnection insulated by a dielectric material, a barrier material surrounding the interconnection, and a via and a trench formed in the dielectric material to the interconnection in accordance with an embodiment of the invention.

Figure 2 shows the substrate of **Figure 1** after the further processing step of patterning a barrier layer to overly the surface of the dielectric material and the side walls of the via and trench and to overly the copper interconnection line in accordance with an embodiment of the invention.

Figure 3 shows the substrate of **Figure 1** after the further processing step of introducing a seed material over the top surface of the dielectric and predominantly along the side walls of the via and trench in accordance with an embodiment of the invention.

Figure 4 shows the substrate of **Figure 1** after the further processing step of exposing the underlying interconnection line in accordance with an embodiment of the invention.

Figure 5 shows the substrate of **Figure 1** after the further processing step of forming a copper interconnection in the via and trench in accordance with an embodiment of the invention.

Figure 6 shows the substrate of **Figure 1** after the further processing step of planarizing the upper surface of the substrate in accordance with an embodiment of the invention.

DETAILED DESCRIPTION OF THE INVENTION

The invention relates to a method of forming an interconnection. Compared to prior art interconnections, the invention is useful in one aspect in reducing the resistivity of the interconnection by allowing direct contact between an interconnection and a conductive device, such as an interconnection through a via to an underlying interconnection line.

Figures 1-6 illustrate a process for forming an interconnection over an underlying interconnection line, such as for example, a copper interconnection line. A typical integrated circuit such as a microprocessor chip may have, for example, four or five interconnection layers stacked one on top of the other each insulated from one another by dielectric material. **Figures 1-6** illustrate, for example, the formation of a second interconnection line of such a circuit over and to be electrically connected to a first interconnection line through an interconnection. It is to be appreciated that the method of the invention may be used for various interconnections within an integrated circuit including to circuit devices and other interconnection lines.

Figure 1 illustrates a cross-sectional side view of a portion of a substrate or wafer having a first copper interconnection line 110 formed in dielectric material 120. Only dielectric material 120 and first copper interconnection

line 110 of the substrate are illustrated. Copper interconnection line 110 is, for example, coupled to an underlying device or devices formed in or on a semiconductor substrate. Dielectric material 120 is, for example, silicon dioxide (SiO_2) formed by a tetraethyl orthosilicate (TEOS) or a plasma enhanced chemical vapor deposition (PECVD) source. Dielectric material 120 may also be a material having a low dielectric constant (a "low k" material), including a polymer, as known in the art.

Surrounding copper interconnection line 110 in **Figure 1** is barrier material 130. In this example, barrier material 130 is silicon nitride (Si_3N_4) deposited to a thickness of approximately 10-50 nanometers (nm) generally depending on the desired characteristics of the barrier layer (e.g., diffusion barrier characteristics). Barrier material 130 may also serve, in one embodiment, to protect copper interconnection line 110 from oxidation (e.g., during oxygen plasma etching) following the patterning of copper interconnection line 110.

Figure 1 shows via 140 through dielectric material 120 to expose barrier material 130. **Figure 1** also shows trench 145 formed in a portion of dielectric material 120 over via 140. A trench and a via may be cut according to known techniques by, for example, initially using a mask, such as a photoresist mask, to define an area for the opening and etching the via with a suitable etch chemistry, such as, for example, a CH_3/CF_4 or C_4F_8 etch chemistry for SiO_2. The mask may then be removed (such as

by an oxygen plasma to remove photoresist) and a second mask patterned to define an area for a trench opening. A subsequent etch forms the trench and the second mask is removed leaving the substrate shown in **Figure 1**.

Figure 2 shows the substrate of **Figure 1** after the further processing step of depositing barrier material 150 over the exposed surface of dielectric layer 120 and in via 140. Barrier material 150 is deposited to a thickness of approximately 10-50 nm depending on the desired characteristics of the barrier material. For example, barrier material 150 is chosen, in one embodiment, to be effective to inhibit conductive material diffusion, such as copper diffusion into dielectric material 120. Barrier material 150 is also chosen, in this embodiment, to have sufficiently different etch characteristics than a seed material that will be applied subsequently. Suitable barrier material 150 includes, but is not limited to, Si_3N_4 and TiN. As will become apparent from the discussion below, in one embodiment, barrier material 150 is chosen to be of the same material as barrier material 130.

Figure 3 shows substrate 100 after the further processing step of depositing seed material 160 over the top surface of substrate 100 and predominantly along the side walls of via 140 and trench 145. Seed material 160 is used, in one sense, in a subsequent electroplating process to form an interconnection in via 140 and trench 150. While barrier material 150 may be a conductive material such as a titanium compound that may be

capable of carrying a current that may be utilized in the electroplating process, barrier material 150 is generally not a good conductor and may cause non-uniform current flow which, in turn, may adversely effect the electroplating process and the reliability of the fabricated integrated circuit. Seed material 160, on the other hand, generally provides uniform current flow during electroplating. Moreover, seed material 160 provides enhanced adhesion of the subsequently formed interconnection to the substrate.

In one embodiment, seed material is, for example, a copper material deposited using standard sputter deposition techniques. Due to the inherent characteristics of the sputter deposition process, the thickness of the deposited copper is shown to be approximately 100 percent, 40 percent, and 5 percent, of the target thickness of seed material 160 on the top surface of substrate 100, the side walls of via 140, and the bottom of via 140, respectively. Thus, by proper targeting of the deposited seed material 160, on the top surface of substrate 100, an insignificant amount of seed material is deposited on the bottom surface of via 140 (i.e., over barrier material 150 at the base of via 140). Thus, in one aspect, the invention seeks to provide a sufficient amount of seed material 160 to seed an interconnection while minimizing the amount of seed material that is deposited at the base of via 140.

Figure 4 shows the subsequent processing step of etching barrier material 150 and barrier material 130 from the base of

via 140 to expose underlying copper interconnection line 110. In this example, seed material 160, properly targeted to minimize the amount of material in the bottom of via 140, acts as a mask during the etching of barrier material. Thus, as noted above, in one embodiment, the material chosen for barrier material 150 and barrier material 130 should have sufficiently different etch characteristics than seed material 160 such that seed material 160 may act as a mask to protect barrier material 150 along the wall or walls of via 140 and trench 145. In the example where barrier material 150 and barrier material 130 are each Si_3N_4, a fluorine chemistry in the presence of energetic argon ions may be used to selectively etch barrier material 150 and barrier material 130 and maintain seed material 160 on the top surface of substrate 100 and along the side wall or walls of via 140 and trench 145. It is to be appreciated that any insignificant amount of seed material 160 deposited at the base of via 140 in the deposition described above may be removed during the selective etch of barrier material 150 and barrier material 130. **Figure 4** shows that once the etching of barrier material 150 and barrier material 130 is complete, underlying copper interconnection line 110 is exposed.

Figure 5 shows substrate 100 after the subsequent processing step of filling via 140 and forming a subsequent copper interconnection line 170 by, for example, a conventional copper electroplating process. By way of example, metallic ions in a pH neutral copper-based solution, such as a copper sulfate-

based solution, may be reduced to a metallic state by applying current between seed material 160 and an anode of an electroplating cell in the presence of the solution. Copper metal becomes deposited onto seed material 160 to fill via 140 and form copper interconnection line 170.

Figure 5 shows that continuous interconnection lines may be formed on a substrate and connected directly to one another without an intervening barrier material layer as is done in the prior art. In this manner, the resistivity of each interconnection is reduced, the resistivity of the interconnection lines is reduced, and the resistivity of an integrated circuit formed according to the methods described above is reduced relative to prior art methods.

Figure 6 shows substrate 100 after the further processing step of planarizing the top surface of substrate 100. The planarization step may be accomplished, for example, by a chemical-mechanical polish as known in the art. In this embodiment, the planarization step proceeds to dielectric material 120 thus substantially removing barrier material and seed material present on the upper surface of dielectric material 120.

The above method of the invention has been described with respect to inventive modifications to a damascene process. It is to be appreciated that the method of the invention has equal applicability to other interconnection formation processes,

including the process described in the U.S. Patent Application Serial No. 09/001,349. Exemplary of that process is the use of a lithographic or masking step to define the interconnection line. Thus, for example, the portion of the top surface of the dielectric that is not covered with photoresist will provide a conductive path to the electroplating solution. Therefore, the interconnection line formed by the electroplating process will overly a portion of the top surface of the dielectric. Using the techniques of the invention, the interconnection line will be directly coupled to an underlying circuit device, including an underlying interconnection line, without an intervening barrier material.

The above method of forming an interconnection has been described with respect to copper interconnections and copper interconnection lines. It is to be appreciated that similar processing techniques may be used for other interconnection materials, including, but not limited to, aluminum alloy interconnections. The invention describes an integrated circuit and a method of producing an integrated circuit utilizing interconnections with reduced resistivity as compared to prior art interconnections having intervening barrier layers between interconnections.

In the preceding detailed description, the invention is described with reference to specific embodiments thereof. It will, however, be evident that various modifications and changes may be made thereto without departing from the broader spirit

and scope of the invention as set forth in the claims. The specification and drawings are, accordingly, to be regarded in an illustrative rather than a restrictive sense.

CLAIMS

What is claimed is:

1. A method of forming an interconnection, comprising

introducing a barrier material in a via of a dielectric to a circuit device on a substrate in such a manner to deposit the barrier material on the circuit device;

introducing a seed material into said via in a manner that leaves the barrier material overlying the circuit device substantially exposed;

substantially removing the barrier material overlying the circuit device; and

introducing a conductive material in the via to form the interconnection.

2. The method of claim 1, wherein the step of introducing a seed material comprises sputter depositing the seed material into the via.

3. The method of claim 1, wherein the barrier material comprises etch characteristics such that the barrier material may be selectively etched in the presence of the seed material.

4. The method of claim 1, wherein the circuit device is an interconnection line.

5. The method of claim 1, wherein the step of introducing the conductive material comprises electroplating.

6. A method of forming an interconnection on a substrate, comprising:

providing a substrate having a circuit device, a dielectric material overlying the circuit device having a via through the dielectric to the circuit device;

depositing a barrier material in the via to substantially cover the side walls of the via and the circuit device;

introducing a seed material into said via in a manner that leaves the barrier material overlying the circuit device substantially exposed;

substantially removing the barrier material overlying the circuit device; and

introducing a conductive material in the via to form the interconnection.

7. The method of claim 6, wherein the step of introducing a seed material comprises sputter depositing the seed material.

8. The method of claim 7, wherein the step of introducing a seed material comprises introducing the seed material over a portion of a top surface of the dielectric material and an amount of seed material over the barrier material overlying the

circuit device is about five percent or less of the amount overlying the top surface of the dielectric.

9. The method of claim 6, wherein the barrier material comprises etch characteristics such that the barrier material may be selectively etched in the presence of the seed material.

10. The method of claim 6, wherein the circuit device is an interconnection line.

11. The method of claim 6, wherein the step of introducing a conductive material comprises electroplating.

12. An integrated circuit comprising:

a substrate having a circuit device;

a dielectric material overlying the circuit device with a via formed in the dielectric material to the circuit device;

a barrier material substantially lining a wall or walls of the via;

a seed layer overlying the barrier material and substantial lining the wall or walls of the via; and

a conductive material directly contacting the circuit device.

13. The integrated circuit of claim 10, wherein the circuit device is an interconnection line

14. The integrated circuit of claim 10, wherein the conductive material is copper.

ABSTRACT

A method of forming an interconnection that includes introducing a barrier material in a via of a dielectric to a circuit device on a substrate in such a manner to deposit the barrier material on the circuit device, introducing a seed material into the via in manner that leaves the barrier material overlying the circuit device substantially exposed, substantially removing the barrier material overlying the circuit device, and introducing a conductive material into the via to form the interconnection.

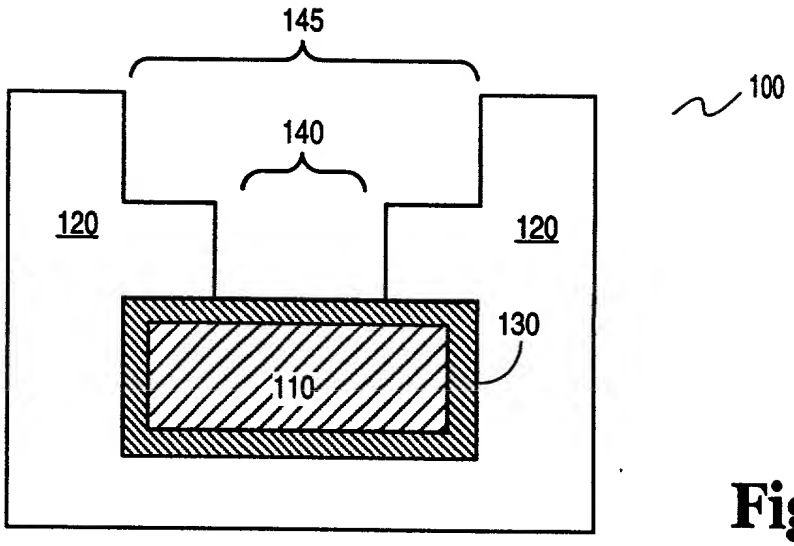

Fig. 1

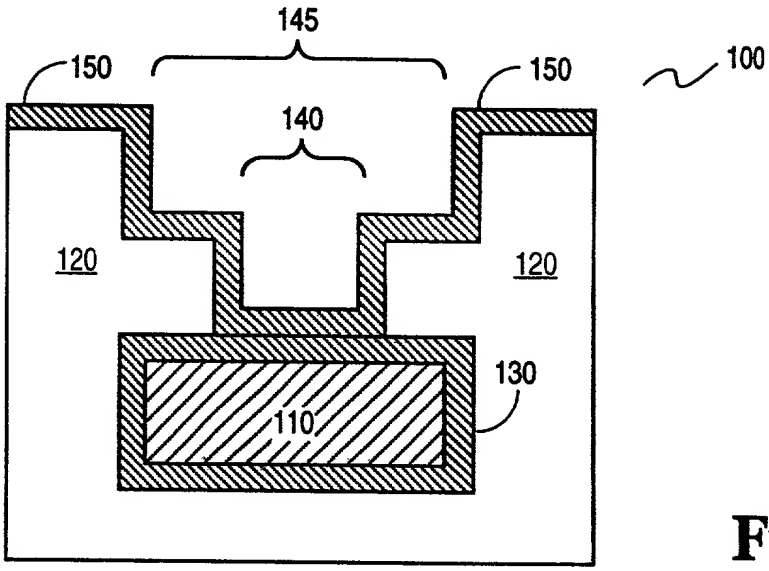

Fig. 2

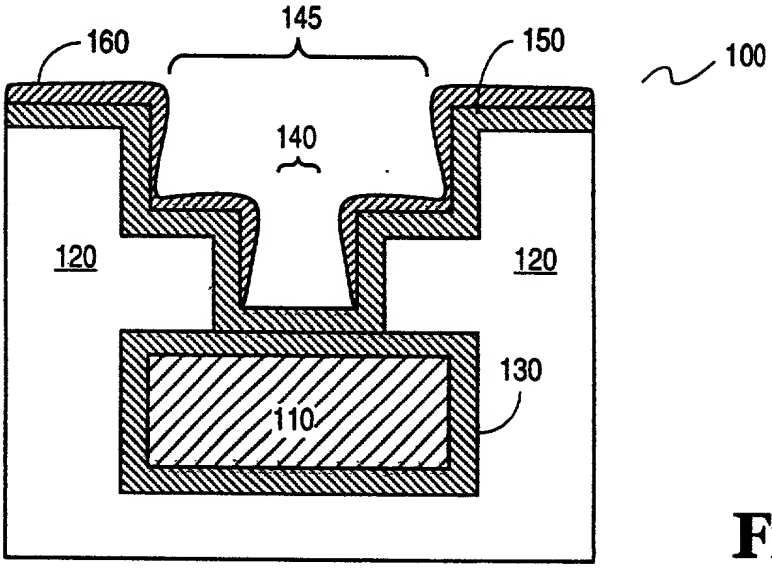

Fig. 3

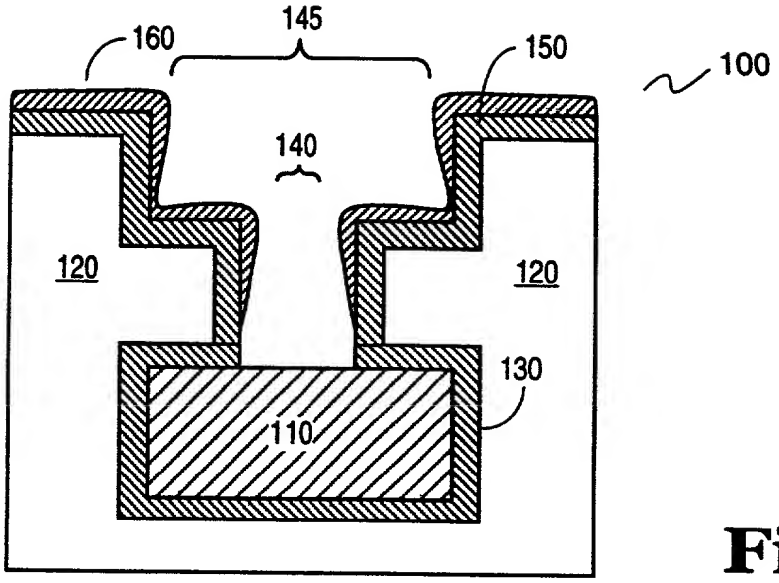

Fig. 4

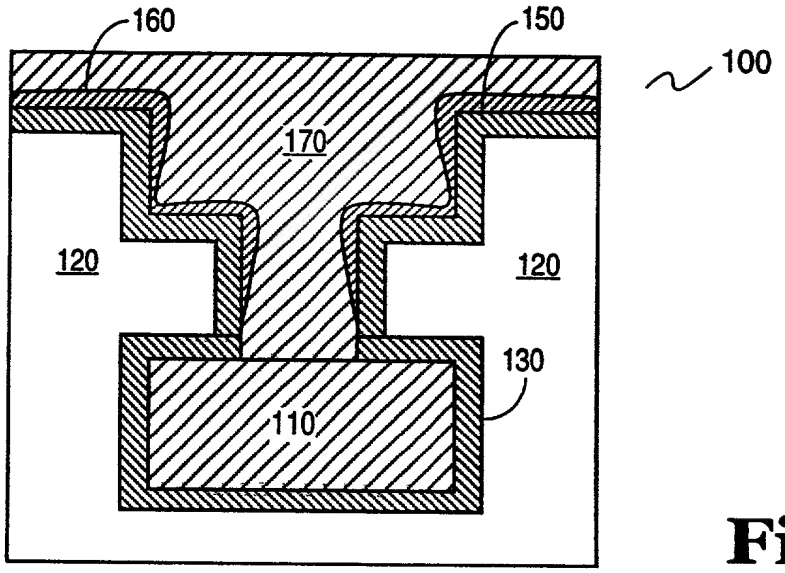

Fig. 5

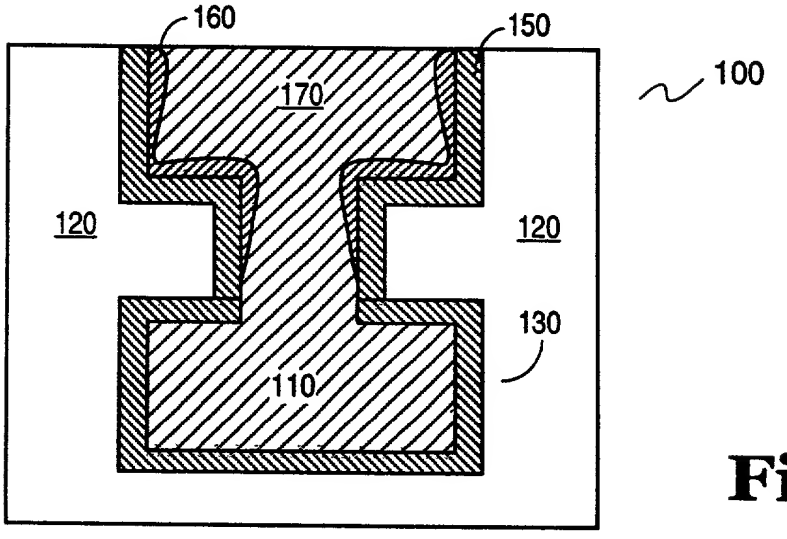

Fig. 6

Attorney's Docket No.: 042390.P6126

DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION (FOR INTEL CORPORATION PATENT APPLICATIONS)

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below, next to my name.

I believe I am the original, first, and sole inventor (if only one name is listed below) or an original, first, and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

A Process to Manufacture Continuous Metal Interconnects

the specification of which

☒ is attached hereto.
☐ was filed on _____ as
United States Application Number _____
or PCT International Application Number _____
and was amended on _____
(if applicable)

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claim(s), as amended by any amendment referred to above. I do not know and do not believe that the claimed invention was ever known or used in the United States of America before my invention thereof, or patented or described in any printed publication in any country before my invention thereof or more than one year prior to this application, that the same was not in public use or on sale in the United States of America more than one year prior to this application, and that the invention has not been patented or made the subject of an inventor's certificate issued before the date of this application in any country foreign to the United States of America on an application filed by me or my legal representatives or assigns more than twelve months (for a utility patent application) or six months (for a design patent application) prior to this application.

I acknowledge the duty to disclose all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, Section 119(a)-(d), of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Prior Foreign Application(s):

APPLICATION NUMBER	COUNTRY (OR INDICATE IF PCT)	DATE OF FILING (day, month, year)	PRIORITY CLAIMED
			☐ No ☐ Yes
			☐ No ☐ Yes
			☐ No ☐ Yes

I hereby claim the benefit under Title 35, United States Code, Section 119(e) of any United States provisional application(s) listed below:

APPLICATION NUMBER	FILING DATE

I hereby claim the benefit under Title 35, United States Code, Section 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, Section 112, I acknowledge the duty to disclose all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application:

APPLICATION NUMBER	FILING DATE	STATUS (ISSUED, PENDING, ABANDONED)

I hereby appoint BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN, a firm including: Farzad E. Amini, Reg. No. 42,261; Aloysius T. C. AuYeung, Reg. No. 35,432; William Thomas Babbitt, Reg. No. 39,591; Carol F. Barry, P41,600; Jordan Michael Becker, Reg. No. 39,602; Bradley J. Bereznak, Reg. No. 33,474; Michael A. Bernadicou, Reg. No. 35,934; Roger W. Blakely, Jr., Reg. No. 25,831; Gregory D. Caldwell, Reg. No. 39,926; Kent M. Chen, Reg. No. 39,630; Lawrence M. Cho, Reg. No. 39,942; Yong S. Choi, Reg. No. P43,324; Thomas M. Coester, Reg. No. 39,637; Roland B. Cortes, Reg. No. 39,152; Barbara Bokanov Courtney, Reg. No. P42,442; William Donald Davis, Reg. No. 38,428; Michael Anthony DeSanctis, Reg. No. 39,957; Daniel M. De Vos, Reg. No. 37,813; Tarek N. Fahmi, Reg. No. P41,402; James Y. Go, Reg. No. 40,621; Richard Leon Gregory, Jr., P42,607; Dinu Gruia, Reg. No. 42,996; David R. Halvorson, Reg. No. 33,395; Thomas A. Hassing, Reg. No. 36,159; Phuong-Quan Hoang, 41,839; Willmore F. Holbrow III, Reg No. P41,845; George W Hoover II, Reg. No. 32,992; Eric S. Hyman, Reg. No. 30,139; Dag H. Johansen, Reg. No. 36,172; William W. Kidd, Reg. No. 31,772; Tim L. Kitchen, Reg. No. P41,900; Michael J. Mallie, Reg. No. 36,591; Paul A. Mendonsa P42,879; Darren J. Milliken, P42,004; Thinh V. Nguyen, Reg. No. 42,034; Kimberley G. Nobles, Reg. No. 38,255; Michael A. Proksch P43,021; Babak Redjaian, Reg. No. 42,096; James H. Salter, Reg. No. 35,668; William W. Schaal, Reg. No. 39,018; James C. Scheller, Reg. No. 31,195; Anand Sethuraman, Reg. No. P43,351; Charles E. Shemwell, Reg. No. 40,171; Maria McCormack Sobrino, Reg. No. 31,639; Stanley W. Sokoloff, Reg. No. 25,128; Allan T. Sponseller, Reg. No. 38,318; Geoffrey T. Staniford, P43,151; Judith A. Szepesi, Reg. No. 39,393; Vincent P. Tassinari, Reg. No. 42,179; Edwin H. Taylor, Reg. No. 25,129; George G. C. Tseng, Reg. No. 41,355; Lester J. Vincent, Reg. No. 31,460; John Patrick Ward, Reg. No. 40,216; Stephen Warhola, P43,237; Charles T. J. Weigell, Reg. No. P43,398; Ben J. Yorks, Reg. No. 33,609; and Norman Zafman, Reg. No. 26,250; my attorneys; and Amy M. Armstrong, Reg. No. P42,265; Robert Andrew Diehl, Reg. No. P40,992; James A. Henry, Reg. No. 41,064; and Edwin A. Sloane, Reg. No. 34,728; my patent agents, with offices located at 12400 Wilshire Boulevard, 7th Floor, Los Angeles, California 90025, telephone (310) 207-3800, and Alan K. Aldous, Reg. No. 31,905; Joseph R. Bond, Reg. No. 36,458; Richard C. Calderwood, Reg. No. 35,468; Sean Fitzgerald, Reg. No. 32,027; James E. Jacobson, Jr., Reg. No. 31,626; Seth Z. Kalson, Reg. No. 40,670; Naomi Obinata, Reg. No. 39,320; Thomas C. Reynolds, Reg. No. 32,488; Howard A. Skaist, Reg. No. 36,008; and Raymond J. Werner, Reg. No. 34,752; my patent attorneys, of INTEL CORPORATION with full power of substitution and revocation, to prosecute this application and to transact all business in the Patent and Trademark Office connected herewith.

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(Name of Attorney or Agent) (Name of Attorney or Agent)

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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